PATENT
5298-17100/SMS03003

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:
Jenne et al.

Serial No.: 10/809,134

Filed: March 24, 2004

For: MAGNETIC MEMORY ARRAY ARCHITECTURE

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Group Art Unit: 2827

Examiner: Le. T.

Atty. Dkt. No.: 5298-17100

CERTIFICATE OF MAILING
37 C.F.R. § 1.18

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DECLARATION UNDER 37 C.F.R. § 1.131

Commissioner for Patents
Washington, D.C. 20231

I, Frederick B. Jenne, hereby declare and state that:

1. I am a named inventor in the above-identified patent application, which is U.S. Patent Application No. 10/809,134 filed on March 24, 2004.

2. I have been informed that in the present application certain claims have been rejected in reference to U.S. Patent No. 6,947,315 to Iwata, which was issued on September 20, 2005, was first published on October 7, 2004, and was filed on November 7, 2003.

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CONCEPTION

3. As supported below, I, along with Eugene Y. Chen, Thomas M. Mnich and William Stevenson, conceived of the subject matter claimed in the present application within the United States before November 7, 2003. The subject matter includes a device including a magnetic random access memory (MRAM) array and a storage circuit distinct from the MRAM array which includes one or magnetic elements. The storage circuit is configured to store parameter settings characterizing applications of current to operate the MRAM array within the one or more magnetic elements.

4. Exhibit A attached hereto is a true copy of pages outlining the invention which bear a date before November 7, 2003. Exhibit B attached hereto is true copy of an email memorandum with an electronic copy of Exhibit A attached. The email memorandum was sent prior to November 7, 2003. The actual dates of the pages outlining the invention and email memorandum have been redacted.

5. Pages 11-13 of Exhibit A describe and illustrate the subject matter of the presently claimed case. In particular, page 12 of Exhibit A illustrates a block diagram of a circuit architecture including MRAM arrays and circuitry for operating the MRAM arrays. Page 13 of Exhibit A illustrates a more detailed block diagram of data routes and control signal routes for accessing the MRAM arrays illustrated on page 12 and specifically includes a block denoting a MTJ configuration latch and another block denoting non-volatile MTJ control data latches. Lines 10-13 on page 11 of Exhibit A states an MRAM MTJ control latch may be used to store settings to operate an MRAM array coupled thereto.

REDUCTION TO PRACTICE AND DILIGENCE

6. From at least a time just prior to November 7, 2003 through the filing of parent U.S. Patent Application No. 10/809,134 filed on March 24, 2004, plans were undertaken to prepare the captioned patent application, which was commissioned to Kevin Daffer at Conley Rose, P.C. I did not abandon, suppress, or conceal the ideas set forth in the claimed invention during at least

the time beginning just prior to November 7, 2003 through the filing of the parent application on March 24, 2004.

7. Upon information and belief, it is my informed understanding that diligence in reducing the invention to practice was therefore maintained from at least as early as just prior to November 7, 2003 through the filing of the parent application on March 24, 2004.

8. I hereby declare that all statements made of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

Frederick B. Jenne

Date: 01/02/06

Exhibit A

MRAM Architecture For Optimized Operation (Revision D)

Fred Jenne
Eugene Chen
Tom Mnich
Bill Stevenson

REDACTED

Exhibit A

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SILICON MAGNETIC SYSTEMS

Summary Of MRAM Architecture Features

Architecture

- **Adjustable Write Pulse Timing**
  - Optimizes write Switching Yield & Reliability By Pulse Width & Pulse Delay Control
- **Adjustable Write Current Amplitude Control**
  - Optimizes Write Current Set Point Between Select & Disturb Operating Window
- **Independently Adjustable Bit Line North & South Write Current Amplitude Control**
  - Accounts For Interlayer Coupling Allowing For Higher Yield
- **Adjustable Temperature Controlled Write Current Amplitude**
  - Modifies Program Current Amplitude To Keep It Centered In Operating Window Over Operating Temperature Range
- **Margin Mode**
  - Finds Weak Bits To Improve Reliability
- **Adjustable MTJ Stress Bias Control**
  - Finds Weak Bits By Voltage Stress Of MTJ Tunnel Junction Improving Reliability
- **DC Write Mode**
  - Allows Measurement Of Write Current To Aid In The Determination Of Write Switching Distributions And Determining Optimum Write Current Settings
- **Write Protect Mode**
  - Prevents Writing Bad Data Into The MRAM Memory During Low Out Of Specification Supply Voltage
- **Non-volatile MTJ Control Data Latch**
  - Replaces Fuses & Metal Mask Options To Hold Data For The Dynamically Optimized Adjustable MRAM Parameters Reducing Manufacturing Costs

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Adjustable Pulse Width & Delays *Architecture*

- The dynamic probability of switching characteristics of the MTJ device are a function of the current pulse widths and delays. There are two current write pulses that control the programming of an cross point MTJ memory device. A Digit line pulse is applied first to rotate the magnetic spin vectors so they are easier to switch. A delayed second Bit line pulse switches the magnetic spin vectors to the opposite state. Generally the longer the current pulse width the higher the probability of switching. If the probability of switching is not high enough one will get a write failure and the reliability of the MRAM suffers. If the pulse widths are longer than required then the access time of the memory in degraded. Hence one would want to be able to set the write current pulse widths to get the required probability of switching yield, but not any longer such that the access time of the memory is pushed out. If the delay between Digit and Bit line pulses is not long enough then the spin vectors are not rotated sufficiently before the Bit line pulse is applied and one can experience a write failure resulting in reduced reliability. If the delay is longer than that required then the access time of the memory is degraded. Hence it is desired to adjust the delay enough to get the required probability of switching but not any further where the access time of the memory is pushed out.

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Adjustable Pulse Amplitude Architecture

- For a cross point memory the selected MTJ device is written by the intersection of the half select Digit line and Bit line current pulses. Other devices not selected can potentially be disturbed by the current pulses along the Digit line, or the current pulses along the Bit line. There is a Digit and Bit line current pulse amplitude window where the yield is optimum. The write current pulses have to be large enough to write (switch) the selected MTJ, but not be large enough to disturb (switch) the non-selected MTJ's. The windows are functions of process variables, such as variations in free layer thickness, MTJ feature size plus others. As an example it is known that the required switching current varies with MTJ feature size. If the current pulse amplitudes are not in the middle of the window between select and disturb, the yield will be degraded. Hence it is desirable to be able to adjust the current pulse amplitudes on the memory chip to optimize yield to account for process variables.

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Independent Adjustable North & South Bit Line Write Current Pulse Amplitudes

Architecture

- The MTJ's switching characteristics are modified by what is termed as the interlayer coupling field. The interlayer coupling is a function of process variables and can vary between wafer to wafer and die to die. The interlay coupling field (Neél coupling as an example) can reduce the amplitude of the current required to switch the free layer in one direction, but increase the required switching current amplitude in the reverse direction. This results in the optimum write current switching window between select and disturb to different for the North versus the South case. If the North and South Bit line switching current amplitudes can be adjusted separately, then the interlayer coupling offset can be eliminated or significantly reduced. This allows the North and South current pulse amplitudes to be optimized to provide a higher yield. Hence it is desirable to be able to adjust the Bit line North and South current pulse amplitudes independently on the MRAM chip.

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Temperature Controlled Write Current Amplitude

Architecture

- The MTJ free layer can be switched at a lower field at high temperature relative to low temperature. The temperature coefficient might be -11%/100 Degree centigrade. If the write current pulse amplitude does not track with temperature, then it will not track the optimum current pulse amplitude switching point in the window between select and disturb. This will result in degraded yield or reliability. Hence it is desirable to provide an on chip circuit to adjust the write current pulse amplitude with temperature.

REDACTED

Margin Mode

- The resistance of an MTJ is low when the free layer is switched to the parallel state and high when switched to the anti-parallel state. The read sensing signal window from the MTJ is derived from the difference in resistance between these two states. A fixed bias voltage is applied across the MTJ resistors and the difference in current is sensed and compared. The difference in resistance can vary with process variables, and defects, resulting in a read failure if the current sensing window becomes to small. The difference between the MTJ sense current, and the reference trip point current is the margin current window. During testing of the MRAM some of these read failures may escape if they are right on the edge of failure and have no margin to the window. By introducing a method to measure the current window, one can eliminate the weak MTJ's and improve the reliability of the MRAM memory. Hence it is desirable to add a margin mode circuit to the MRAM chip.

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Adjustable MTJ Bias Voltage *Architecture*

- The resistance of the MTJ is a function of the bias voltage across the tunnel junction. The maximum sense signal from the MTJ's has an optimum bias voltage for a given circuit implementation. The optimum bias voltage may vary with process variables. For a fixed bias voltage the read signal may not be optimum and successful read yield may be degraded. If the bias voltage can be adjusted to account for process variations the yield may be improved. Hence it is desirable to add an adjustable bias voltage circuit on the MRAM chip. In addition, the MTJ tunnel junction will break down prematurely if the applied bias if high enough. Normally the applied bias is designed to be well below this breakdown value providing high reliability. However there may be defects in the tunnel junction that cause the breakdown voltage to be low resulting in read failures with time, and may escape testing. The tunnel junction breakdowns can be accelerated by increasing the bias voltage across the junction. Weak tunnel junctions will break down much sooner than good junctions, and weak tunnel junctions can be caught at test or burn-in. Hence it is desirable to add an adjustable bias circuit to accelerate tunnel junction breakdowns and improve MRAM reliability.

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DC Write Mode

- The probability switching distribution needs to be known to set the write current amplitude to optimum yield conditions. The probability switching distribution may vary from wafer to wafer or die to die with process variables. To determine the probability switching distributions on a die requires that the write switching current amplitude be determined during testing. As an example during the write operation, the current (I_{Supply}) of the die can be monitored. The difference between I_{Supply} before and after write is the write current. Hence it is desirable to add a write current test mode that enables monitoring the write current during test.

REDACTED

Write Protect

- If the MRAM memory has corrupt data then the memory is unreliable and a system failure may occur. The write operation of an MRAM is guaranteed only over a certain voltage range such as from 4.5 to 5.5V. If a write operation is in progress during a power supply failure and the voltage supply drops below 4.5V, corrupt data may be written into the MRAM memory causing the memory to be unreliable. This can be prevented by monitoring the power supply voltage, and not allowing data to be written into the MRAM when the power supply voltage falls below the minimum operating range. In this example it would be 4.5V. This can be called a write protect operation. This write protect operation can be added to the MRAM chip. Hence it is desirable to add a write protect circuit to the MRAM chip to prevent corrupt data being written into the MRAM during a power supply failure to improve reliability.

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MRAM MTJ Non-volatile Control Latch

Architecture

- Various functions of an MRAM memory would like to be adjustable to improve yield and reliability. Fuses and metal mask options provide this function. However once they have been programmed they generally cannot be changed. It is desirable to adjust various functions dynamically during testing to determine optimum settings. A CMOS latch can perform this function, but when the power is removed the settings are lost. Fuses could be used to retain the settings, but they take up a large area on the chip and add additional manufacturing steps. Using an MRAM MTJ control latch to hold the settings allows testing the MRAM memory to determine optimum settings and then load them into the non –volatile MTJ control latch.

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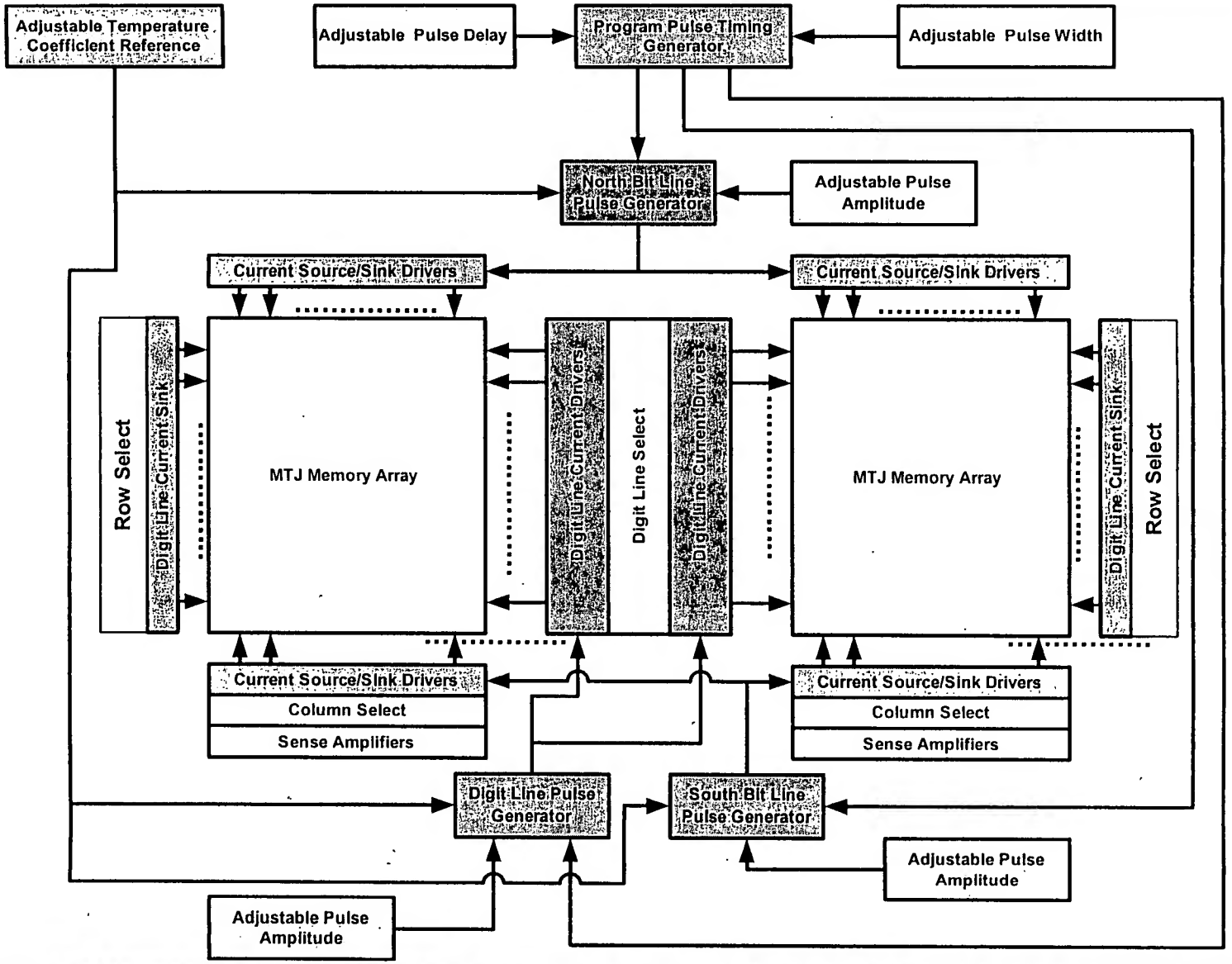
MRAM Adjustable Write Current Pulse Control

Architecture



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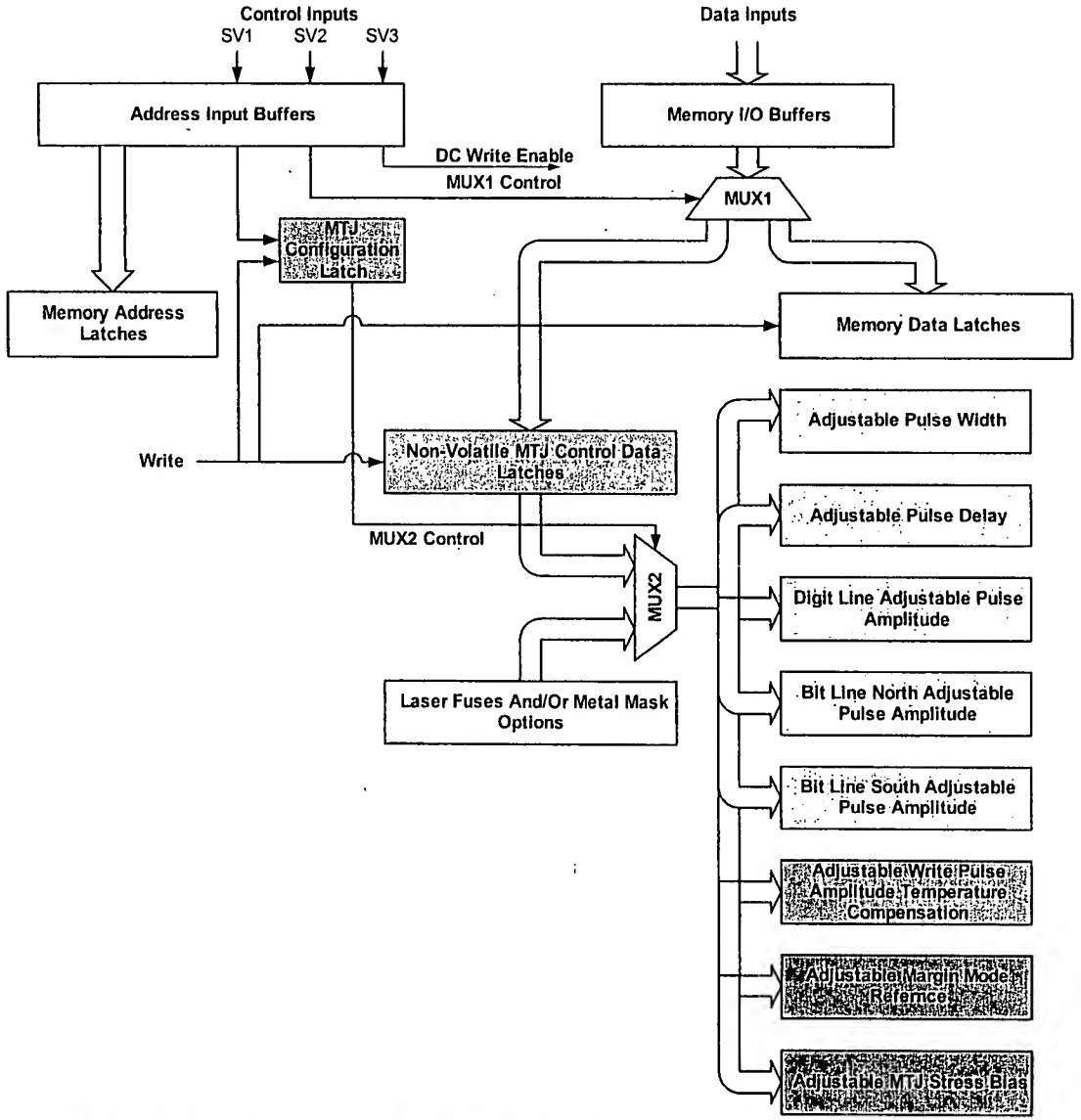
Control Data Block Diagram

Architecture



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MTJ Control Latch Description *Architecture*

- Critical MRAM functions can be dynamically adjusted to determine optimum settings by, and stored in, an MTJ non-volatile control latch. One embodiment is to use super high voltages on the address inputs to control basic functions and the I/O to enter control data. The super voltage inputs override the normal address path and provide control signals. When the address input voltage is raised higher than V_{Supply} plus (say 20%) on a super voltage input, a control signal is enabled. As an example control data is available at the input of the I/O buffers and to MUX1 (The outputs are tri-stated). SV2 directs MUX1 to send data to the Non-volatile MTJ Control Latch. SV1 input is available to the MTJ Configuration Latch which directs MUX2 to choose either data from the Non-volatile MTJ Control Data Latch or from fuses/and or metal mask options. Subsequently a Write signal loads the data or a control signal into the Non-volatile MTJ Control Data Latch and the MTJ Configuration Latch. In this case the MTJ Configuration Latch is loaded with control signal MUX2 Control to choose data from the Non-volatile MTJ Control Data Latch. This data is then sent to the various functions to adjust their parameters. When power is removed the Non-volatile Control Data latch and the Non-volatile MTJ Configuration Latch retains the data in the non-volatile latches. Other embodiments could use other non-volatile control data storage methods such as programmable logic, etc.

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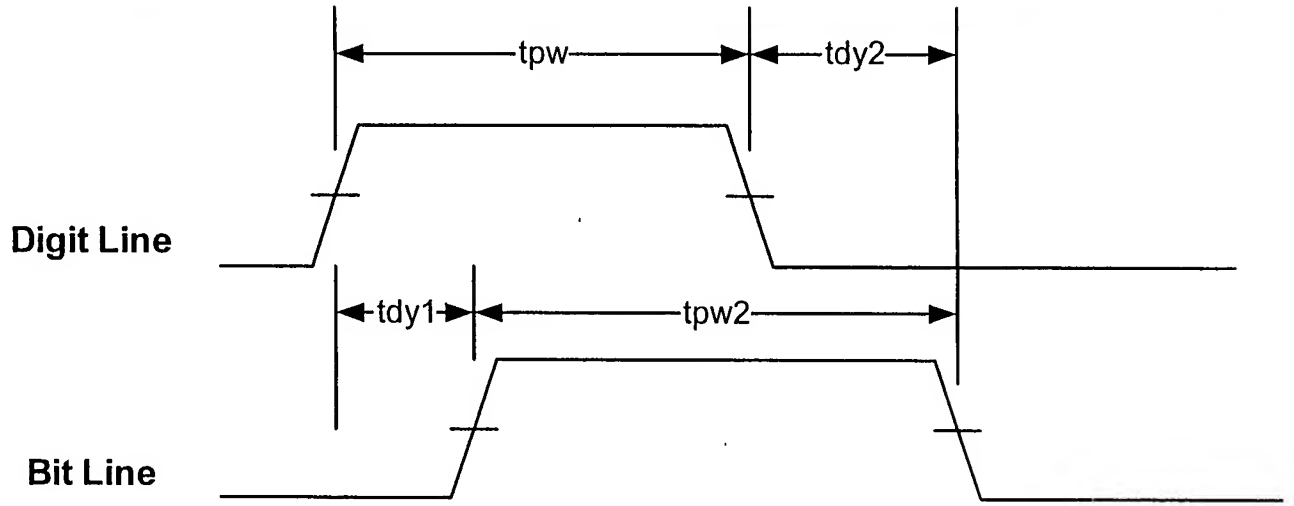
Pulse Generator Timing Control

Architecture



- The pulse generator timing generator allows the delays tdy1 and tdy2 to be adjustable through DAC settings over a range to optimize yield (as an example from 1 to 5ns)
- The pulse generator timing generator allows the pulse widths tpw & tpw2 to be adjustable through DAC settings over a range to optimize yield (as an example from 2 to 30ns)
- The DAC settings ca be controlled by laser fuses, metal mask options, or from data from a NV MTJ latch

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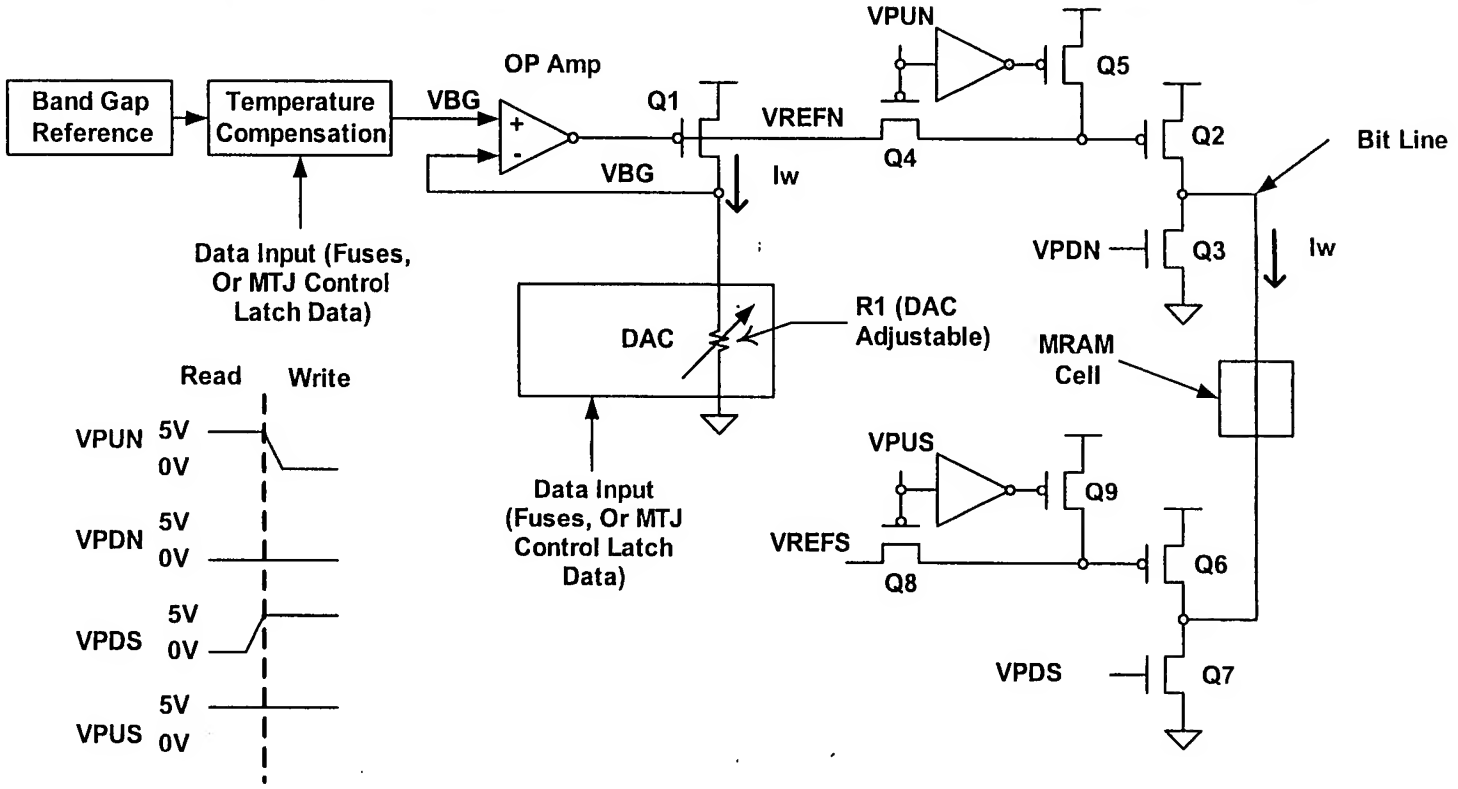
Write Current Amplitude Control Architecture



- The write pulse amplitude is controlled by a reference voltage VREFN applied to the gate of Q1 which supplies current across resistor R1. The voltage across R1 is forced to precision voltage VBG resulting in a current Iw that is adjustable by DAC settings and temperature compensated. This precision current is mirrored through transistor Q2 to the MRAM cells on the bit line. The same methodology is used for controlling the Digit line current. Other methods can be used to control the current amplitude.

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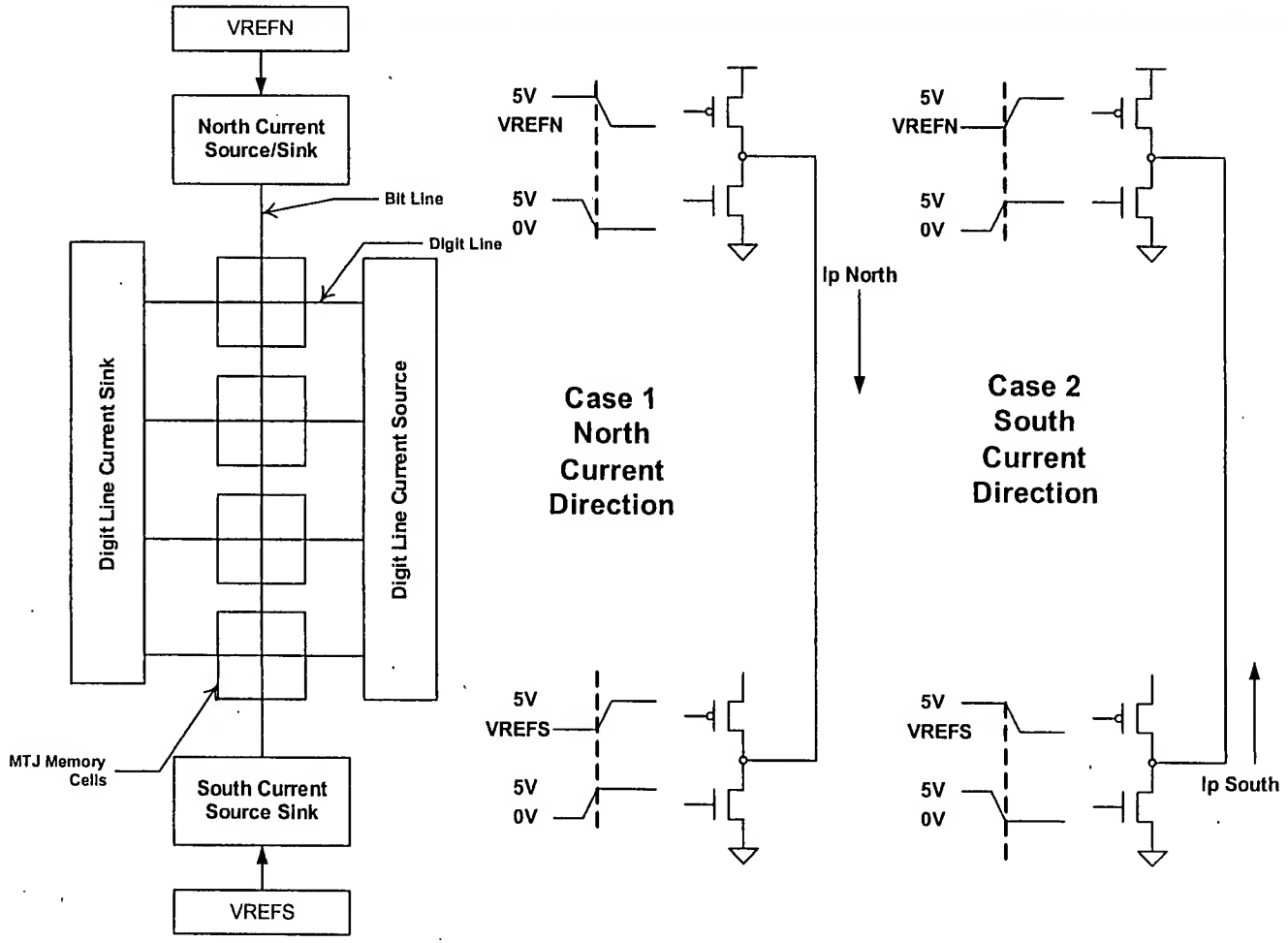
Independent Control Of North & South Bit Line Current *Architecture*



- The North and South Write current pulse amplitudes are independently controlled by their separate reference voltages VREFN & VREFS.

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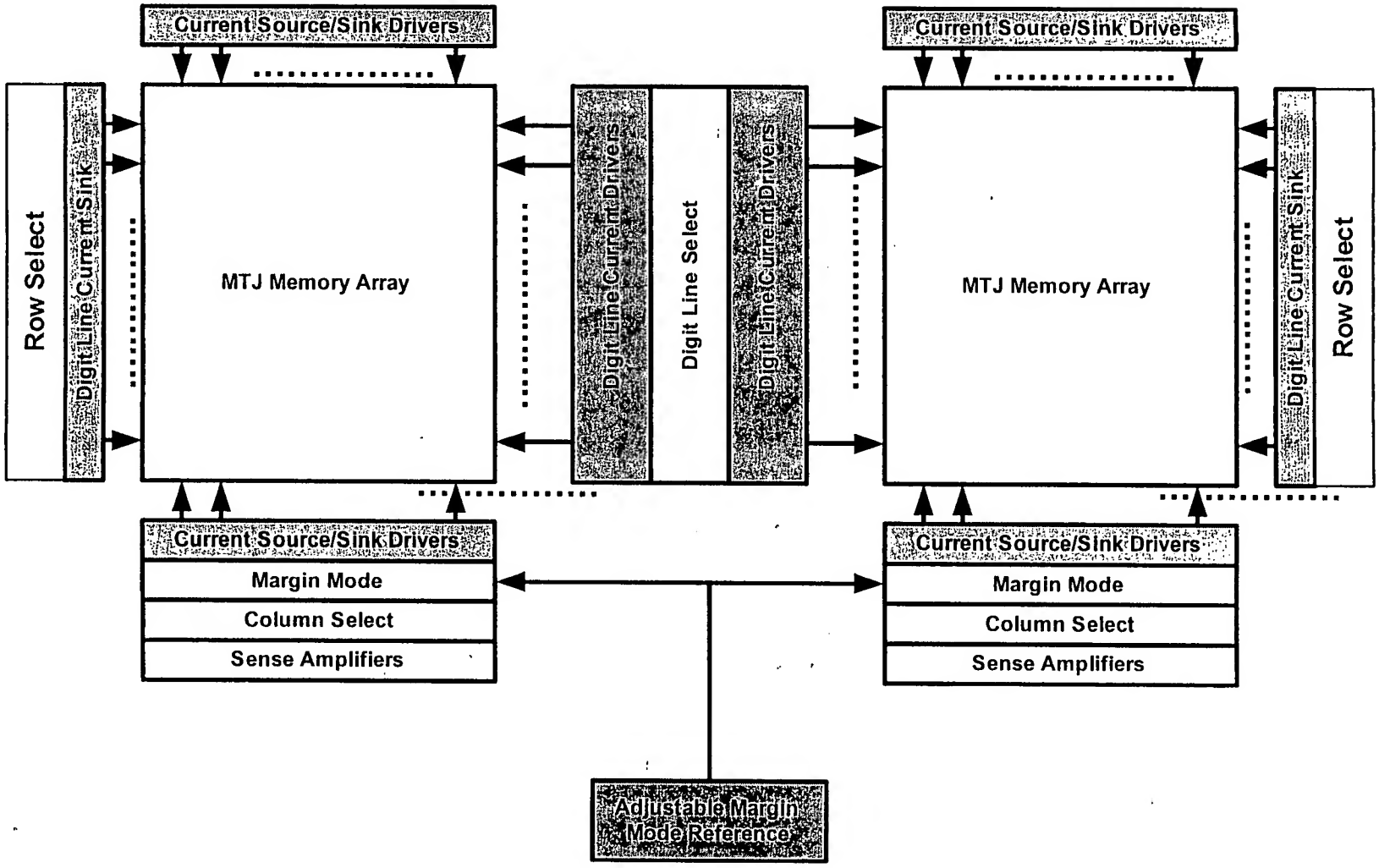
Margin Mode Block Diagram

Architecture



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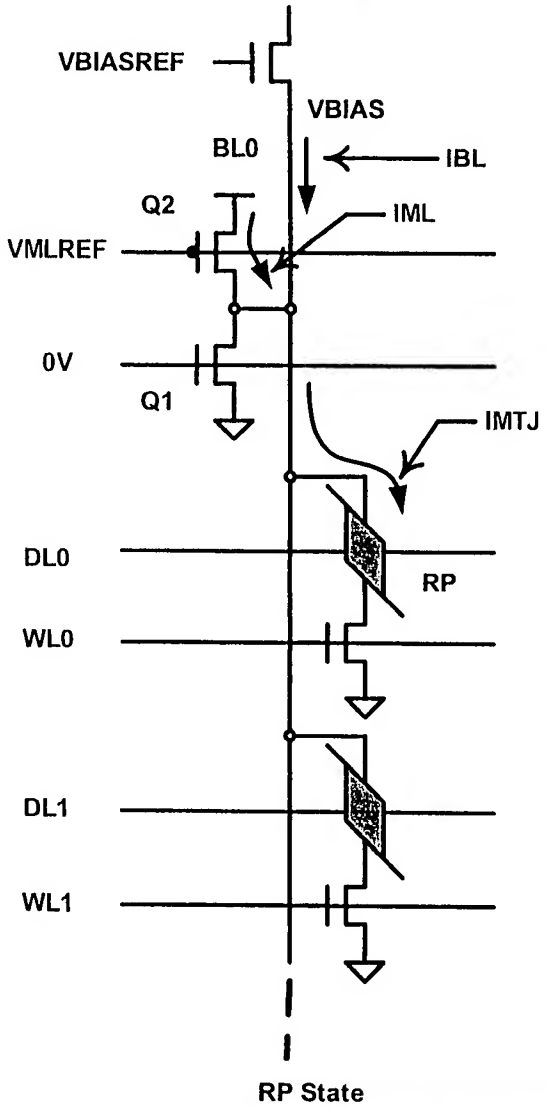
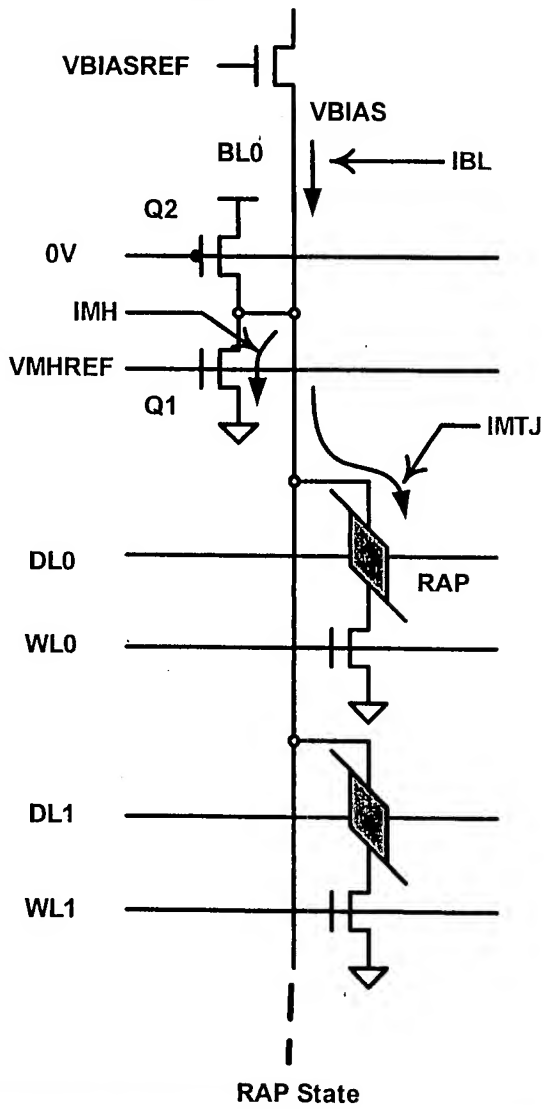
Margin Mode Circuit

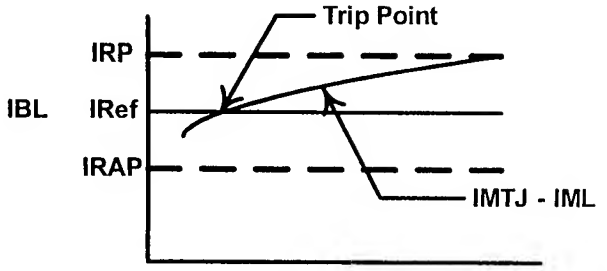
Architecture



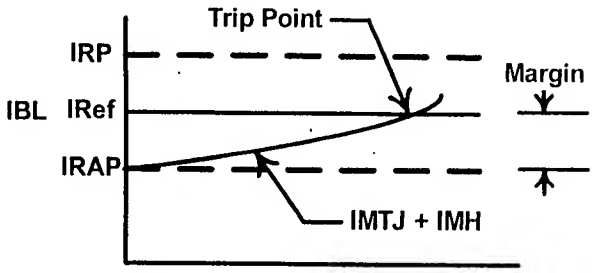
RP State



RAP State



VMLREF (RP State)



VMHREF (RAP State)

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Margin Mode Description

Architecture

- The current from the MTJ in the "1" state or "0" state is compared against a reference current that has a value somewhere in between the two. The difference between the "1" state or "0" state and the reference current is defined as the margin current window. The MTJ (Cell A) is being read and other cells on BL0 are turned off. By subtracting a known current from BL0 when the MTJ is in the "0" state (Low resistance parallel) at the point of failure (Reference trip point current reached) one can determine the current margin window. This is done by applying a reference voltage VMHREF to transistor Q1 such that a trip point failure occurs. The current through Q1 at trip point is the difference between the "0" state and trip point current or the margin window. The same applies to the case where the MTJ is in the "1" state (High resistance anti-parallel) except that transistor Q2 and VMLREF are used to add current to the bit line to cause a failure. The current through Q2 is the margin window current.

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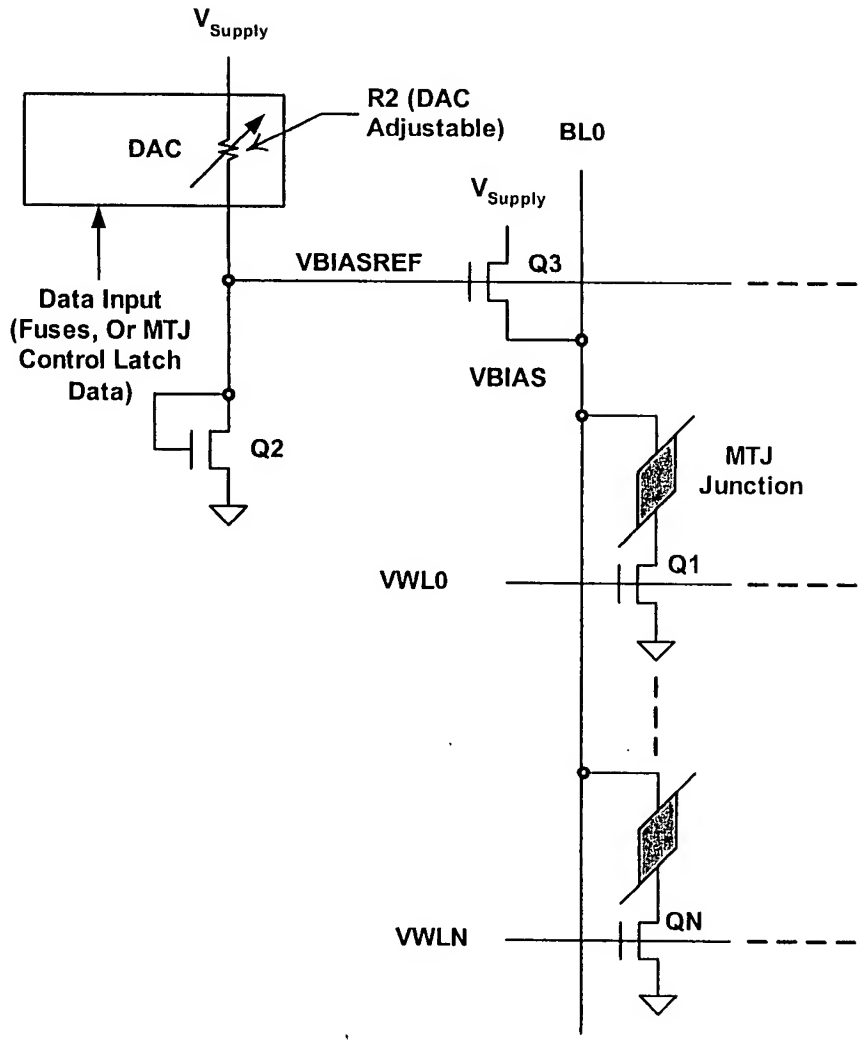
Adjustable MTJ Stress Bias

Architecture

- During normal read operation the bit line bias voltage is supplied through transistor Q3 by applying a bias reference voltage on it's gate (Say 400mV). If the transistor (Q1) resistance is 25% of the MTJ resistance then the bias across the MTJ would be 300mV. The normal break down of the MTJ junction might be 1.4 to 1.9V and has high reliability. However there might be MTJ junctions that have defects and have breakdown voltages below 1.4V. Using voltage acceleration factors one can detect weak junctions at test or burn-in. VBIASREF can be generated by the impedance ratio between the diode connected transistor Q2 and resistor R2. The resistor R2 is part of a DAC and adjusted by inputs from fuses, metal mask options, or the MTJ non-volatile latch. During stress test the fuse and metal mask options can be overridden by the MTJ non-volatile latch and can be dynamically changed.



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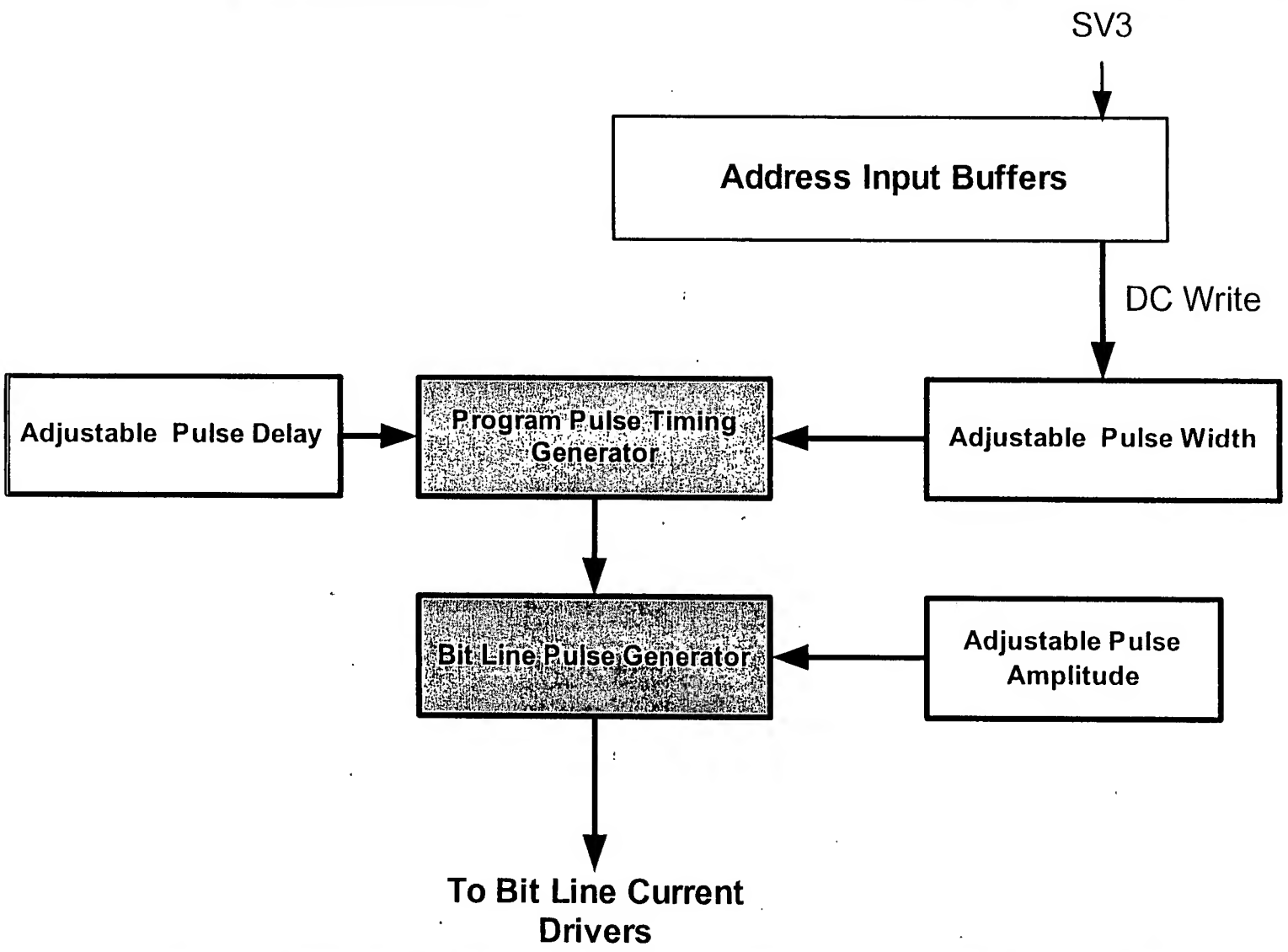
DC Write Mode

Architecture



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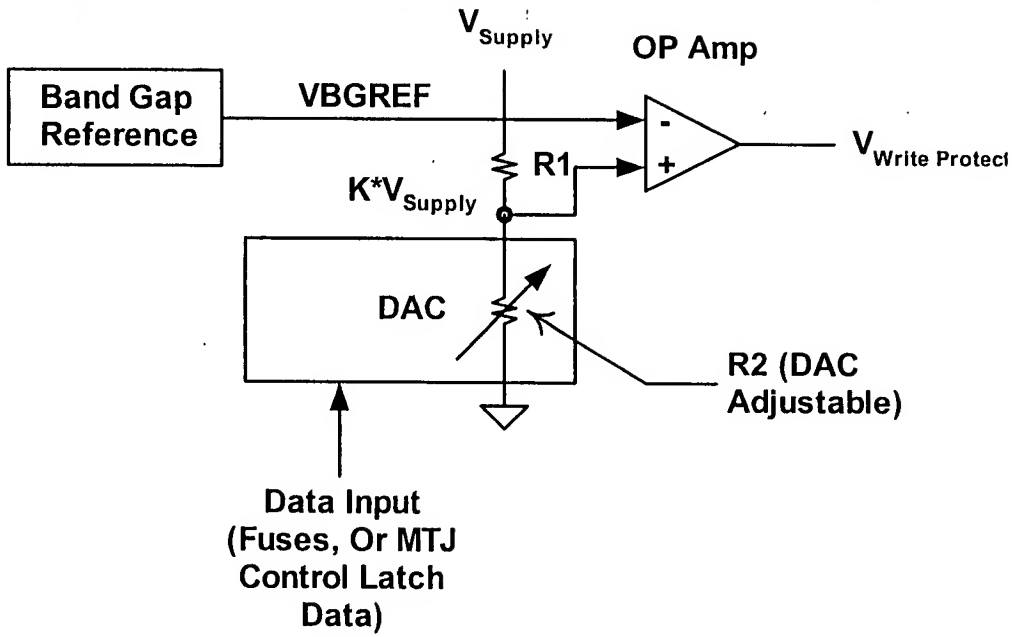
Write Protect Mode



- During the Write operation when V_{Supply} drops below a critical value (say 4.5V), bad data may be written un-intentionally into the MRAM memory. This is averted by preventing a write operation when V_{Supply} drops below a critical level (say 4.5V). This may be implemented by ratioing down V_{Supply} by some factor K and comparing it to a precision band gap voltage reference VBGREF with an OP Amp. The K factor is the ratio of R1/(R1+R2). R2 is part of a DAC and can be adjusted by inputs from fuses, metal mask options, or non-volatile MTJ control latch data. Hence the desired critical trip point is adjustable. When the trip point is reached the voltage from the Op Amp $V_{Write Protect}$ prevents a write operation.

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SILICON MAGNETIC SYSTEMS

Claims

Architecture

- MRAM Memory With Adjustable Write Pulse Width Timing
- MRAM Memory With Adjustable Write Pulse Delay Timing
- MRAM Memory With Adjustable Write Pulse Amplitude
- MRAM Memory With Separate Adjustable North & South Bit Line Write Pulse Amplitude
- MRAM Memory With Temperature Compensated Write Pulse Amplitude
- MRAM Memory With Adjustable Temperature Compensated Write Pulse Amplitude
- MRAM Memory With Margin Mode
- MRAM Memory With Adjustable MTJ Bias Voltage
- MRAM Memory With MTJ Stress Bias Above Normal Operation
- MRAM Memory With Adjustable Stress Bias Voltage
- MRAM Memory With DC Write Mode
- MRAM Memory With Write Protect Mode
- MRAM Memory With Adjustable Write Protect Mode
- MRAM Memory With A Non-volatile MTJ Control Data Latch
- MRAM Memory With A Non-volatile MTJ Configuration Latch
- MRAM Memory Where Critical Functions Can Be Dynamically Adjusted To Determine Optimum Values
- MRAM Memory Where The Optimized Critical Functions Settings Are Stored In A Non-Volatile MTJ Control Data Latch

REDACTED

Exhibit B

Mollie Lettang

From: Fred Jenne [frj@cypress.com]
Sent: REDACTED
To: Mollie Lettang
Subject: Architecture Rev D

Mollie,

Here is the updated architecture slides revision d.

Fred

Fred Jenne
Vice President Technical Group

Exhibit B

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